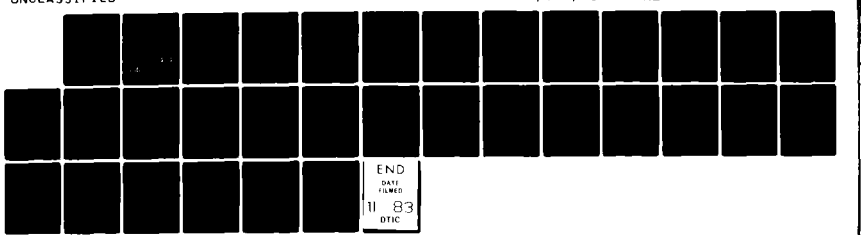
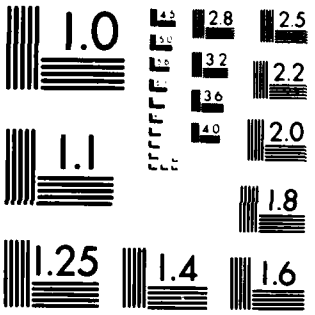
AD-A124 274 PROGRESS ON DIGITAL DOSIMETER(U) NAVAL SURFACE WEAPONS 1/1
CENTER SILVER SPRING MD J L DAVIS ET AL. OCT 82
NSWC/TR-82-456 SBI-AD-F500 121

UNCLASSIFIED F/G 6/18 NL





NSWC TR 82-456

PROGRESS ON DIGITAL DOSIMETER

BY JOHN L. DAVIS, PATRICK J. WINTERS,
BLAND B. HOUSTON

RESEARCH AND TECHNOLOGY DEPARTMENT

OCTOBER 1982

NAVAL SURFACE WEAPONS CENTER

Dahlgren, Virginia 22448 • Silver Spring, Maryland 20910

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER: NSWC TR 82-456	2. GOVT ACCESSION NO.: AD-A124 274
	3. RECIPIENT'S CATALOG NUMBER:
4. TITLE (and Subtitle): PROGRESS ON DIGITAL DOSIMETER	5. TYPE OF REPORT & PERIOD COVERED: Interim
	6. PERFORMING ORG. REPORT NUMBER:
7. AUTHOR(s): John L. Davis; Patrick J. Winters; Bland B. Houston	8. CONTRACT OR GRANT NUMBER(s):
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Naval Surface Weapons Center (Code R45), White Oak, Silver Spring, MD 20910	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62766N; F66512 ZF66512001; R02AD002
11. CONTROLLING OFFICE NAME AND ADDRESS:	12. REPORT DATE: October 1982
	13. NUMBER OF PAGES: 33
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office):	15. SECURITY CLASS. (of this report): UNCLASSIFIED
	15a. DECLASSIFICATION/ DOWNGRADING SCHEDULE:

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Dosimeters
Alpha Counters
Radiation Damage
Memory Devices
Integrated Circuits
Transient Radiation Effects
Dynamic Random Access Memories

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Recent work on the source of errors in D-RAMs suggests that they might become the basis for a practical digital dosimeter. We carried out a series of experiments to determine if commercially available D-RAMs can function as alpha counters in conventional digital circuits. We exposed a 64K D-RAM to a weak alpha source while operating it as part of a minicomputer memory. Comparison of the errors produced with the counts produced by a good surface barrier detector showed that about 15% of the alpha particles incident on the chip

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE
S/N 0102-LF-014-6601

UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

produced bit flips. Proper programming should double this response. A 16K D-RAM, operated at reduced V_{DD} gave a somewhat lower response rate to alpha radiation. The test set-ups are described and some quantitative data are presented.

FOREWORD

This work was supported by the Independent Exploratory Development Program (IED) at the Naval Surface Weapons Center. The authors wish to express their appreciation to the IED Board for this support.

This work originated in discussions among members of the Nuclear Branch (R41) and the Solid State Branch (R45) about the feasibility of developing a better personnel radiation dosimeter. An initial outcome of these discussions was the preparation of a patent disclosure in mid 1981 on the concept of a digital dosimeter based upon the use of semiconductor memory elements as the sensor, and the appropriate electronics so as to interface with a computer for readout and storage of the exposure information. Subsequently IED funding was sought, and obtained, for exploration of the digital dosimeter. This is the first report of results on this project and presents what is essentially a proof of concept for such a device. Subsequent reports will present our progress towards a practical device.

The work has had the assistance of a number of individuals at the White Oak Laboratory. The authors would like to particularly thank Dr. Donald G. Simons for his aid and for the use of the Van de Graaff facility and Dr. Gordon K. Riel for his discussions of radiation dosimetry problems. We also wish to thank Mr. Patrick K. Cady and Mr. Herman I. Cordova for their very able assistance in setting up and carrying out the 64K irradiation experiments.

Approved by:

I. M. BLATSTEIN, Head
Radiation Division

CONTENTS

ILLUSTRATIONS

TABLES

CHAPTER 1

INTRODUCTION

THE DOSIMETRY REQUIREMENT

There are currently about 100,000 Navy personnel who use dosimeters. Furthermore this number is increasing. These personnel are involved in handling nuclear weapons as well as repairing and operating reactors. To protect these personnel an improved individual dosimetry system is needed which is easy to use, accurate, inexpensive, very reliable and which provides automated output for ease of permanent record keeping.

One of the more widely used dosimeters comprises a thermoluminescent crystal whose light output is proportional to the ionizing radiation to which it had been exposed. To be read, the dosimeter must be taken to a central facility where the crystal can be heated and the light output accurately measured. Such a device is intrinsically an integrator of total radiation received. It can give no indication of the current rate of exposure. Furthermore the reading process takes a significant amount of time. Thus there is a delay between exposure and the measurement of that exposure. As used today, the system has hand kept records which are subject to human errors. Finally, the process is fairly expensive. Because of the problems of accurate dosimetry the Navy relies on massive shielding. This introduces heavy cost and weight penalties. Thus the Navy has a requirement for a dosimetry system that is quicker, more accurate and cheaper than that currently in use. Similar requirements for personnel dosimetry exist at DoE facilities and have been documented in a study by Pacific Northwest Laboratory.[1]

SOFT ERRORS IN SEMICONDUCTOR MEMORIES

The observation and explanation of soft errors in semiconductor memories has suggested a concept for a novel dosimeter which might offer some significant advantages over the present system. A soft error is a mistake in a computer memory which cannot be traced to any permanent defect in the system's components. The memory stores data in binary bits as a zero or a one. When an error occurs the memory gives a zero when it should have given a one or vice versa and we speak of a bit as having been flipped. Thus a soft error is a randomly occurring bit flip which has no apparent cause. Needless to say, this poses a difficult problem for system designers.

---

1. Brackenbush, L. W., and Endres, G. U., "Personnel Neutron Dosimetry at Department of Energy Facilities," Pacific Northwest Laboratory Report PNL-3212, UC-41, August 1980. Available from NTIS, 5285 Port Royal Road, Springfield, VA 22151.

In April 1978, May and Woods[2] proposed an explanation for the soft errors which were becoming a serious problem in dynamic random access memories (D-RAMs). They proposed that the errors were being generated by alpha particles striking the silicon chip on which the D-RAM was constructed. Figure 1 shows a single cell of the D-RAM and indicates the mechanism by which an alpha particle can cause an error. The upper part of the figure shows a single cell. The field electrode is positively charged to the point where, in equilibrium, a significant number of electrons (note that the substrate is p-type and the electrons are minority carriers) are held in the storage region under the electrode. Through the bit line these electrons can be removed leaving the storage region in a non-equilibrium deeply depleted condition. The D-RAM stores zeros and ones with the storage regions being either depletion regions or equilibrium inversion regions depending on the particular address of the individual cell and the design of the chip. The state of the storage region can be sensed through the bit line when the transfer gate is driven positive. Because the depletion region is a non-equilibrium state it will in time decay back to the equilibrium inversion condition. For a usable memory some circuit must periodically sense those cells that are depleted and recharge their storage regions (actually remove any electrons that have leaked in) before enough electrons leak in so that the circuit would sense an inversion. This is called refreshing and is done automatically by circuits on the semiconductor chip when the proper signals are fed in. This refresh requirement is the reason why the memory chips of this type are called dynamic memories or D-RAMs.

The lower portion of the figure shows the energy bands near the surface and indicates the effect of an alpha particle striking the surface. The bands are bent down by the potential on the field electrode. Thus there is an electric field near the surface. Now, if an alpha particle penetrates the silicon, it will lose energy to the silicon, the lost energy appearing as electron-hole pairs. For a 4 MeV alpha, energy is lost at a rate of 150 KeV/micron. Electron-hole pairs require about 3.6 eV each, hence the alpha generates about 4×10^4 electron-hole pairs/micron. Electron-hole pairs generated in the region where the bands are bent will see the electric field and will become separated, the electrons going to the surface, and the holes moving away. Electron-hole pairs that are generated beyond the field region will diffuse at random and a fraction will reach the field region where they will respond to the field and become separated.

If the surface region is inverted, the equilibrium condition, there will be a gradient in electron concentration at the surface and a consequent diffusion current. This diffusion current is just sufficient to balance the current due to the electric field, thereby maintaining the equilibrium situation. In this case the effect of the field on the electron-hole pairs generated by the passing alpha particle will be countered by the diffusion current and the net effect of the alpha will be small. If, however, the surface is depleted there is no diffusion current, the electrons are attracted to the surface and the holes are repelled. Electrons will collect at the surface. This will move the depletion region in the direction of an inversion region. If the process is carried far enough the memory element will have had one of its bits flipped--a soft error will have occurred.

---

2. May, Timothy C., and Woods, M. H., "A New Physical Mechanism for Soft Errors in Dynamic Memories," Proc. 16th Annual Conference on Reliability Physics, IEEE New York, 1978 p. 33.

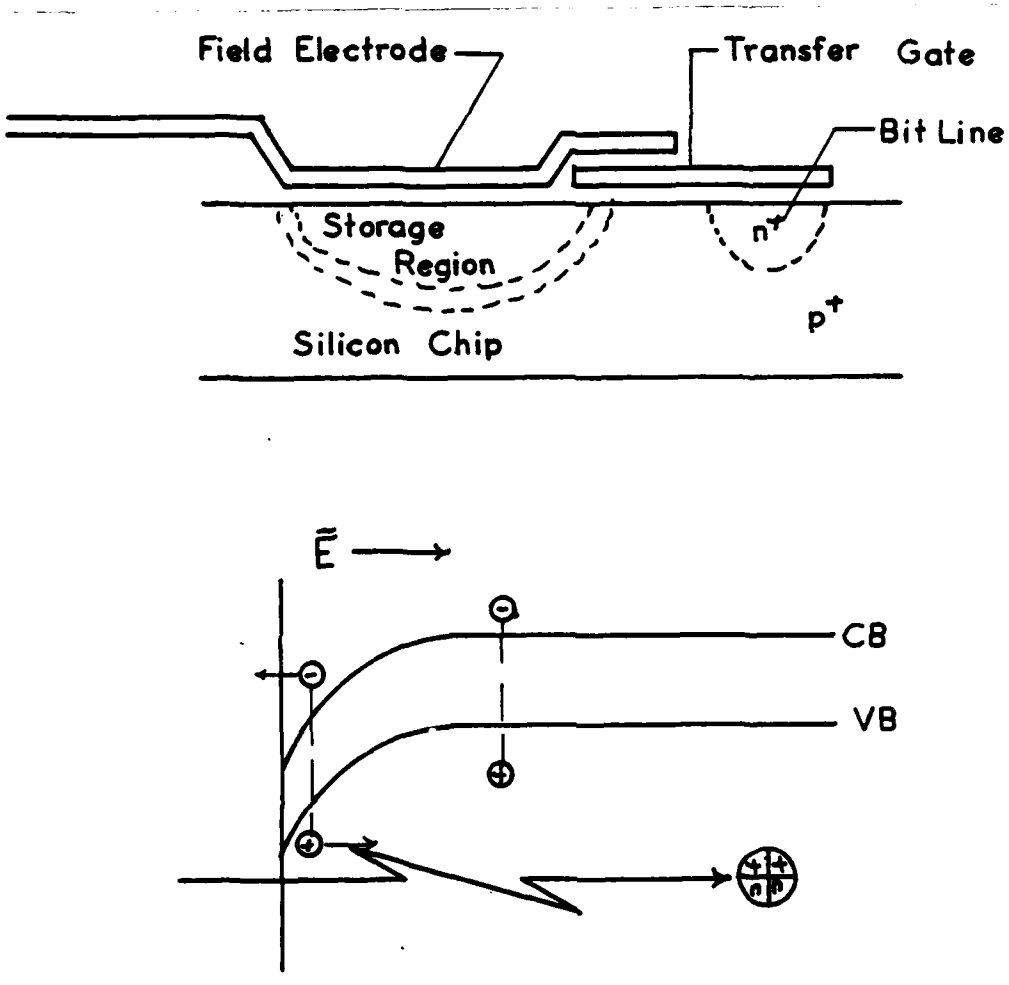


FIGURE 1. SOFT ERRORS IN D-RAMS

May and Woods[2] proposed that the observed soft errors were due to alphas coming from uranium and thorium which are present in the parts-per-million level in the glasses used to make the cases in which the memory chips are mounted. Since then, a number of other workers have confirmed their results and their model is generally accepted. Bouldin and Kumar[3] have reported an analysis of the material used to package the D-RAMs which found up to 2 ppm uranium and up to 1.2 ppm thorium. Gibbons and Pittman,[4] testing packaging materials for alpha emission reported that all the material they tested had some alpha activity, the lower limit being about 0.1 alpha particles per cm^2/hour.

Other authors have investigated the effects of other ionizing radiation on memory chips. Guenzer, Wolichi, and Allas[5] studied 6.5, 9, and 14 MeV neutrons and 32 MeV protons, finding about one bit flip per 10^8 particles/cm^2, a fairly low sensitivity. They also suggested that all parts of the circuit might be sensitive to radiation, not just the memory cells. Wyatt et al[6] examined the effects of protons up to 130 MeV on 4K D-RAMs and found that the higher energy protons would cause both 0-1 and 1-0 transitions. Campbell and Wolicki[7] found that photons in the energy range 15-22 MeV would flip bits in 16K memories. Sivo et al[8] modeled the effects of cosmic rays on static memory devices. Yaney, Nelson and Vanskike[9] investigating 16K devices found that decreasing supply voltages would raise sensitivity, that off normal incidence alphas generated more errors, that the bit lines were sensitive to alphas, and there was a strong maximum in the sensitivity as a function of energy at 3-4 MeV.

---

3. Bouldin, D., and Kumar, A., "Materials Analysis Aspects of the Alpha Particle Induced Error Phenomenon," Proc. 29th Electronics Components Conf., IEEE New York, 1979, p. 265.
4. Gibbons, H. P., and Pittman, J. D., "Alpha Particle Emissions of Some Materials in Electronic Packages," Proc. 29th Electronics Components Conf., IEEE New York, 1979, p. 257.
5. Guenzer, C. S., Wolichi, E. A., and Allas, R. G., "Single Event Upset of Dynamic Rams by Neutrons and Protons," IEEE Trans. on Nuclear Sci., NS-26(6), 5048(Dec. 79).
6. Wyatt, R. C., McNulty, P. J., Toumbas, P., Rothwell, P. L., and Fily, R. C., "Soft Errors Induced by Energetic Protons," IEEE Trans. on Nuclear Sci., NS-26 (6), 4905(Dec. 79).
7. Campbell, A. B., and Wolichi, E. A., "Soft Upsets in 16K Dynamic RAMs Induced by Single High Energy Photons," IEEE Trans. Nuclear Sci., NS-27(6), 1509(Dec. 80).
8. Sivo, L. L., Peden, J. C., Brettschneider, M., Price, W., and Pentecost, P., "Cosmic Ray Induced Soft Errors in Static M.O.S. Memory Cells," IEEE Trans. on Nuclear Sci., NS-26(6), 5042(Dec. 79).
9. Yaney, David S., Nelson, J. T., and Vansskike, Lowell L., "Alpha Particle Tracks in Silicon and Their Effect on Dynamic M.O.S. Reliability," IEEE Trans. on Electron Devices ED-26(1), 10(Jan.79).

The semiconductor manufacturers have responded in three ways. They have used very pure materials to make the cases, thereby removing as much of the uranium and thorium as possible. They have covered the chips, inside the cases, with a protective plastic often a polyimide. Finally, they have developed error correcting codes which will automatically test for errors and correct bit flips each time the memory is read.

In their paper May and Woods used the concept of a critical charge. Basically this is the charge that when added to a depletion region would cause the memory to act as if the region were in inversion resulting in an error. This will be some fraction of the mobile charge in the storage region. An alpha particle of a given energy will generate a fixed number of electron-hole pairs. Also a fixed fraction of these will be collected by a depletion region. Thus the charge introduced into a depletion region by an alpha of a given energy is somewhat fixed. If this charge exceeds the critical charge the bit will be flipped giving a soft error. For these reasons we would expect that the memorys with more and smaller storage cells would be more sensitive to radiation. This is the situation observed. The soft errors did not become a serious problem until the semiconductor industry began to make 16K and 64K dynamic RAMs. We would also expect the critical charge to be reduced if the voltage on the field electrode were reduced. This turned out to be the case in our work.

A DIGITAL DOSIMETER

With the realization that ionizing radiation would produce errors in semiconductor memory chips it was proposed[10] that this vice be made a virtue and the D-RAMs be used as radiation detectors. In 1981 personnel at NSWC proposed that advantage be taken of the digital character of the soft error mechanism and that a fully digital dosimeter be developed. Such a dosimeter would have a number of advantages. Since each incoming alpha particle flips a single bit, the D-RAM is intrinsically a digitally integrating sensor. The background level of spontaneous bit flips is very low--it may be due to the background cosmic ray flux. Thus the dynamic range of a digital dosimeter can be made very high. It can be increased by increasing the range of the counter which is recording the number of flipped bits. A simple, rate calculation repeated at short intervals could be used to actuate an alarm. A block diagram of a simple prototype digital dosimeter is shown in Figure 2. The control and processor load data into the radiation sensitive D-RAM, read it out and record errors in the radiation hardened memory as they occur. The processor also calculates dose rates and will trigger the alarm when the rate reaches a predetermined level. The hardened memory can also contain the identification of the user of the individual dosimeter. The device communicates through the I/O port with an external computer which periodically reads out the memory on the dosimeter and resets the hard memory and which maintains personnel dose records.

A dosimeter of this type would offer a number of advantages such as:

- giving a rate of exposure as opposed to integrated dose.

---

10. Cerofolini, Gianfranco, and Ferla, Giuseppe, "A Proposal: Dynamic RAMs as Particle Detectors," Nuclear Instruments and Methods 169, 125(1980).

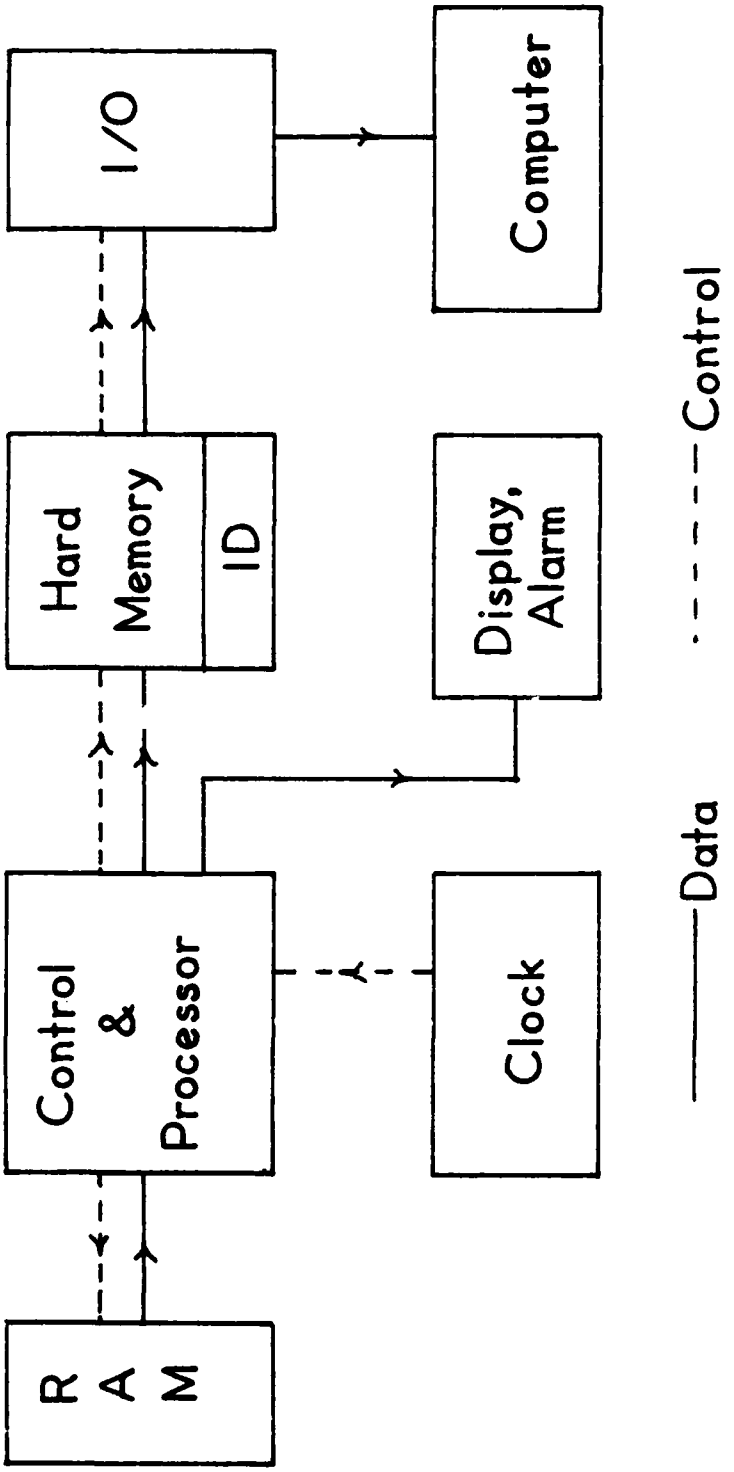


FIGURE 2. BLOCK DIAGRAM OF A DIGITAL DOSIMETER

- providing a possibility of masking different parts of the memory differently to sense different neutron energies.

- a ready means to generate an automated data base of an individuals radiation exposure history which could be filed with other personal characteristics for subsequent analysis e.g., what percentage of a particular crew over 30 have been exposed to a given level of radiation.

The computer that stores the read-out could be any general purpose computer of the types that are available on ships and at all shore facilities. Thus the dosimeter could be read in seconds and an individuals exposure calculated "on the spot". Because of the high dynamic range and the accuracy of hardened memory the accuracy of such a system should be excellent. Finally if it can be based on widely available integrated circuits the cost should be quite low.

To develop such a digital dosimeter a number of steps need to be taken. First we need to demonstrate that commercially available D-RAMs can be used to count alpha particles. Enough data should be taken to determine how consistent these components are with one another. Operating parameters for maximum sensitivity need to be explored. Other types of components should be explored. For example, the charge coupled device (CCD) should be sensitive to alphas for the same reason that D-RAMs are. Since silicon devices are not intrinsically sensitive to neutrons the efficiency of converting neutrons to other forms of radiation which the semiconductors can detect should be explored. Examples are converting energetic neutrons to energetic protons by elastic collision and the emission of alpha particles by boron after capture of thermal neutrons. With this basic information obtained prototype dosimeters can be constructed and an optimal design developed. The research described in this report is the beginning of these steps.

CHAPTER 2

EXPERIMENTAL WORK

INTRODUCTION

The aim of this years' experimental program was to determine if 16K and 64K memory elements could function as alpha particle counters in ordinary digital circuits and if they are sensitive enough to warrant pursuing as the sensitive element in a digital dosimeter. To do this two separate experiments were set up. One of these tested 64K RAMs and the other 16K RAMs.

The two set-ups functioned in slightly different ways. The 64K experiment used the memory chip as an integrating detector. After exposure to radiation it printed out the actual memory adresses of the bits that had flipped upon exposure to alpha particles. The 16K experiment used a counter as a continuous read-out of the number of bits that had flipped. The flipped bits were reset as soon as they were read. In this set-up the voltages to the memory chip under test and the timing of the read-refresh cycle could be varied.

THE 64K EXPERIMENT

This experiment was built around a commercially available microcomputer. This was a model MCPU-800 purchased from Miller Technology of Los Gatos, California. This unit has a ZILOG Z-80 microprocessor for a CPU which is driven at a 4 MHz clock rate. It has 32K bytes of ROM and 64K bytes of RAM. All the components are mounted on a single 4.5 by 7 inch board with STD bus output.

To communicate with the computer we used a Texas Instruments ASR 733, Silent 700, terminal. This terminal uses the RS 232 interface. Therefore we constructed an interface board to change the TTL voltages to the higher RS 232 voltages. We also purchased the Monitor Program for the MCPU-800. This program resides in the 32K ROM.

The 64K byte RAM comprises eight 64K by one bit dynamic RAM chips. The chip that carries the least significant bit was used as the device being tested. We built a header which carries this chip and is connected to the computer board by a sixteen conductor (16 twisted pairs, each with a ground) extension cord. Figure 3 is a block diagram of the experimental set-up.

The alpha irradiation of the 64K chip was carried out in the scattering chamber at the NSWC Van de Graaff accelerator facility. This chamber was evacuated during irradiation so there was no attenuation of the alpha particles by the atmosphere. Alpha particles were provided by an ^{241}Am source. The source and a beam defining aperture were mounted on an arm which could be rotated to point at the several ports

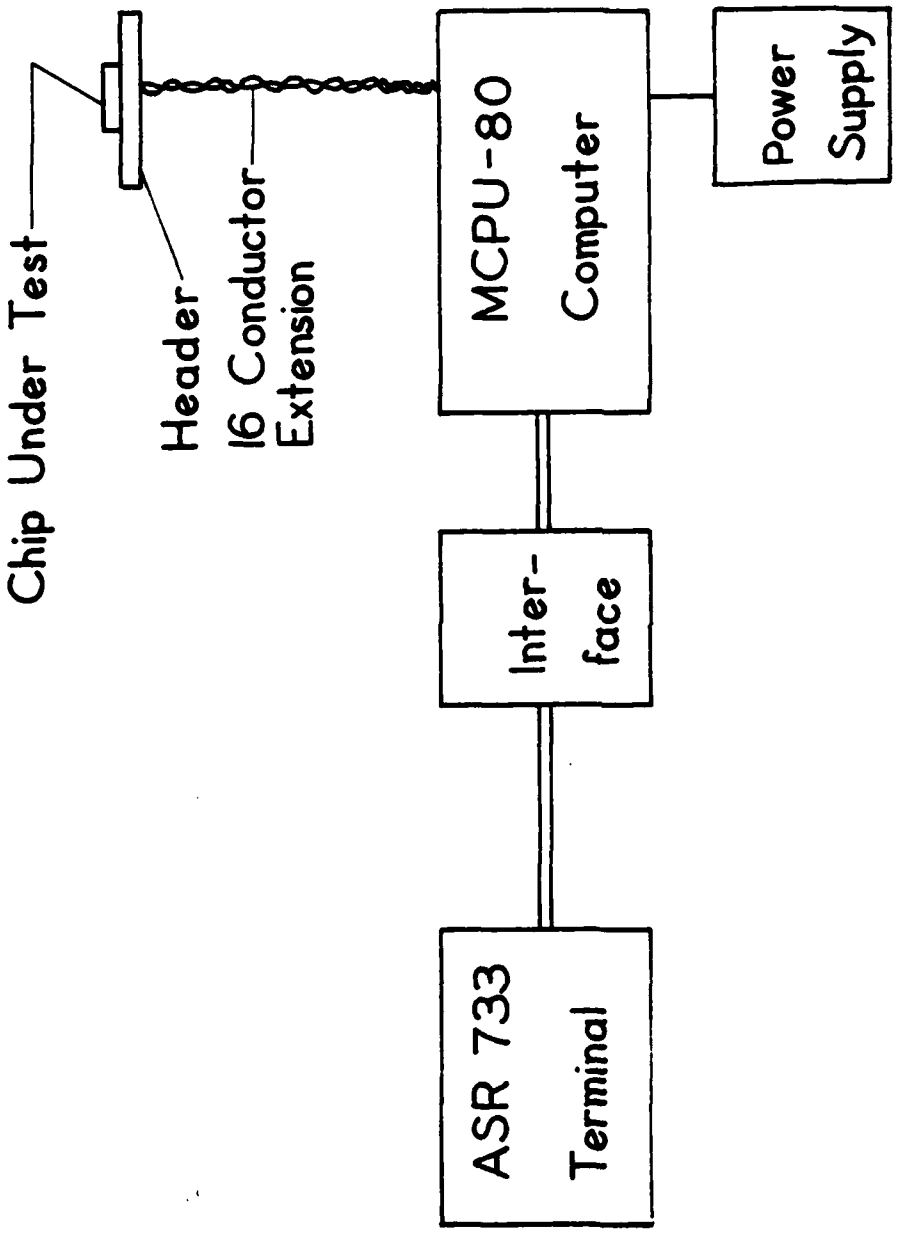


FIGURE 3. BLOCK DIAGRAM 64K EXPERIMENT

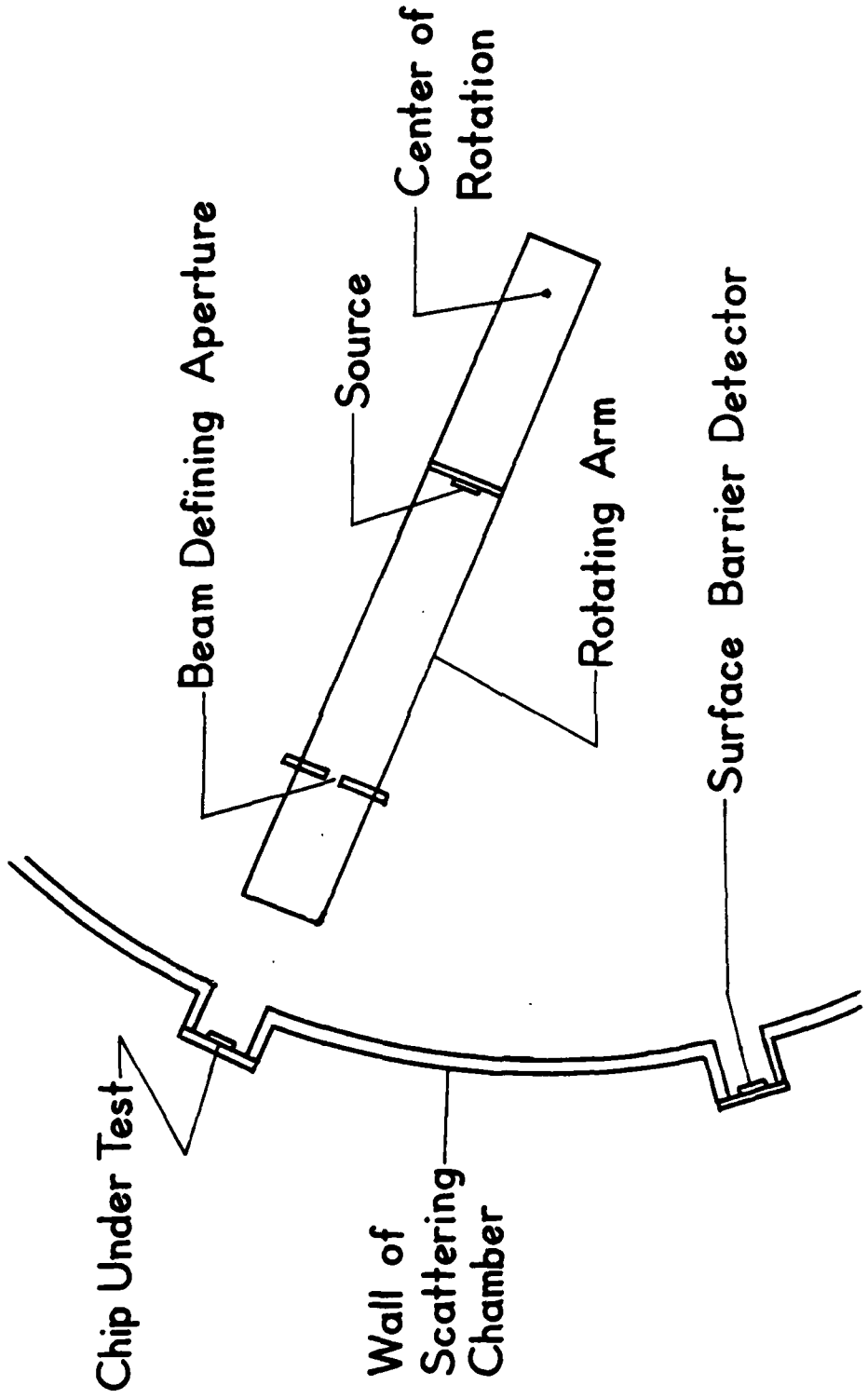


FIGURE 4. 64K IRRADIATION GEOMETRY

of the scattering chamber. In this experiment we compared the detection efficiency of the memory chip with a surface barrier detector. We mounted the chip in its header at one port and the surface barrier detector at another. The geometry of the irradiation process is shown in Figure 4.

The total source strength is 2.384×10^{4} alphas/steradian-second. For the 1 mm aperture used we measured a rate of arrival of alphas with the surface barrier of 13.46 ± 2.3% per minute. We used this value to measure the relative efficiency of the chip with respect to the surface barrier detector.

THE 64K EXPERIMENTAL RESULTS

The 64K chips used in these experiments were Motorola MCM 6665. We obtained specimens from an early production lot that had not been protected from alphas by a polyimide coating. The top was removed by carefully cutting the solder around the top away and then lifting the top with a razor blade. The surface of the silicon chip is divided into four rectangular regions each of these is divided into two roughly square regions. These are the storage cells of the memory. These regions are surrounded by the supporting circuitry, sense-refresh amplifiers and address decoders. Figure 5 shows a schematic of the chip. Each of the four regions comprises the storage cells for consecutively numbered bits. The addresses (in hexadecimal) of the bits in each rectangle are also shown in the figure.

When the monitor program runs it uses memory in the range C000-FFFF. In addition the stack, which the monitor also uses, runs from BFFF to BFB0. Thus storage cells in the left half of the figure are used when the monitor runs. For this reason we aimed the alpha beam at the area in the right half of the figure. The monitor capability to load specific data into a range of addresses and to search a range of addresses for specific data was used to detect the bit flips.

An initial run to test for non-alpha-induced bit flips was made. The command

FILL 00 0000 7FFF

was entered. This loaded the right half of the chip with zeros. Next the computer was left turned on for several weeks. During this time the monitor kept the RAM refreshed but did not change the data or read the data entered. At the end of this period the command

SEARCH 01 0000 7FFF

was entered. This command caused the monitor to cycle through the range of addresses indicated and, whenever it encountered an 01 to print out the address of the 01 on the terminal. This background count rate test was made with the test header out of the Van de Graaff scattering chamber. During this test only two bit flips were detected. Thus the background level of bit flips is very low.

After the background run the test chip in its header was mounted in the scattering chamber port. Two sets of data were taken, the first with zeros loaded in the memory and ones detected and the second with ones loaded and zeros detected. Table 1 is a summary of the results.

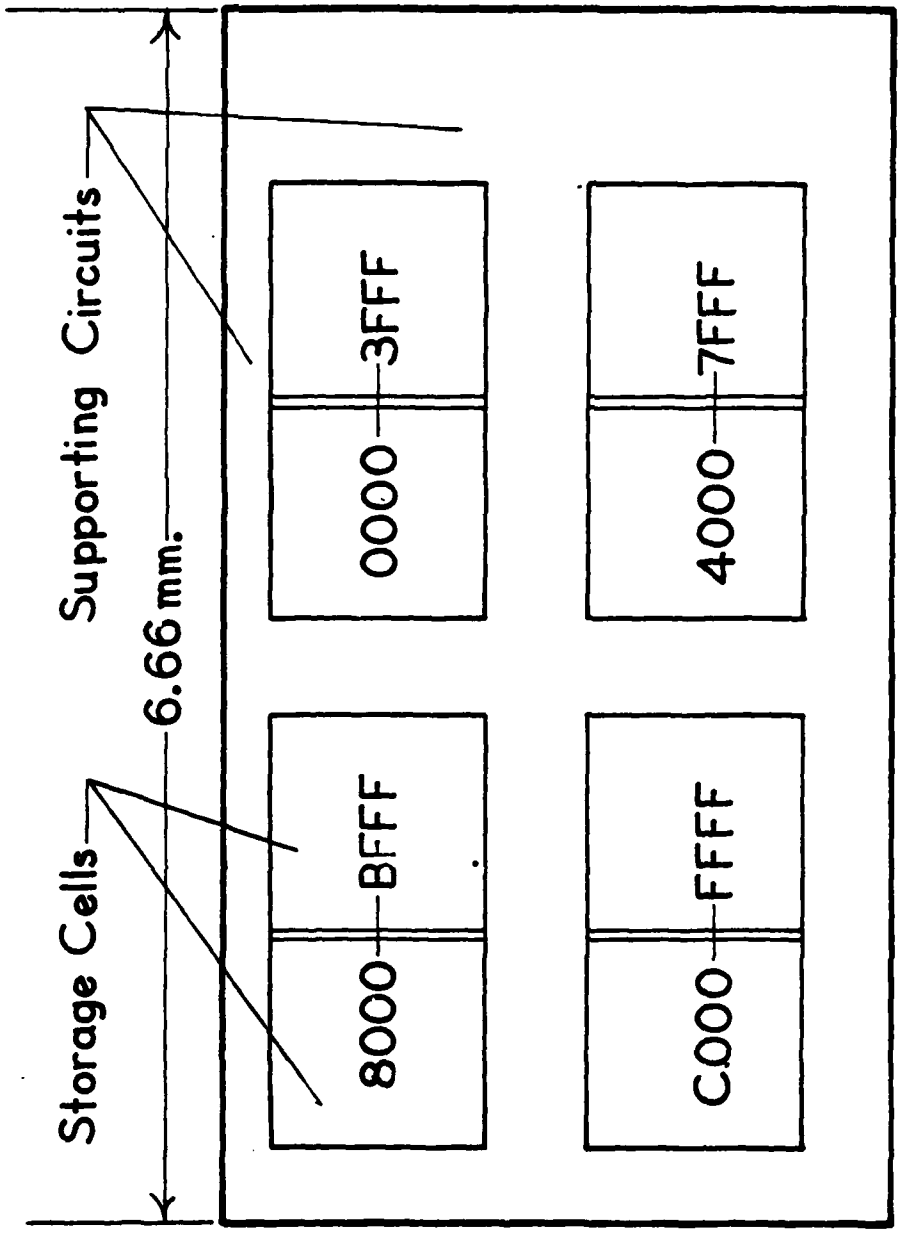


FIGURE 5. MOTOROLA 6665 CHIP

TABLE 1. ALPHA COUNTING DATA FOR 64K D-RAM

Bit Flips	Exposure Time (min)	Flips Detected	Rate (flips/min)	Error
0-1	990	1960	1.98	2.3%
1-0	1363	1819	1.33	2.3%
Surface Barrier Detector			13.46	2.3%

These results indicate that the 64K RAM is an effective alpha particle counter. The very low background rate of errors show that the RAM has a very large dynamic range. We would expect that the 0-1 and 1-0 bit flip rates should be very close, closer than we have observed here. This is because in exactly half of the addresses in the RAM 1's are stored as depletion regions and in the other half (store 1's) as inversion regions. Thus, whether one loads 0's or 1's one has put half of the cells in a condition to be sensitive to radiation. The 0-1 bit flip rate is 14% of the surface barrier detector count rate. The latter detector is assumed to be 100% efficient. Thus we conclude that the RAM is 15% efficient as an alpha particle detector. This less-than-100% efficiency may well be due to geometrical factors such as the beam of alphas spreading beyond the sensitive regions of the RAM. Much more important is the fact that only half of the cells are in the depletion state. If we loaded all the cells into the depletion state we might expect that the observed efficiency would double, giving a value of about 30%.

THE 4K-16K EXPERIMENT

Because of their larger critical charge we expected that the 4K and 16K D-RAMs would prove less sensitive to alpha particles. For this reason we designed this experiment so the operating voltages and the refresh rate could be changed at will. With this capability we can search for the operating parameters which give the greatest sensitivity to radiation.

Figure 6 shows a block diagram of the experiment. We built it around a memory tester which is based on a design proposed by Lockhart.[11] The rate of operation is set by the master oscillator, a Waveteck Model 144 HF Sweep Generator. We built the memory tester from standard TTL integrated circuits which are driven by the 5 volt power supply. The three variable voltages, V_{BB}, V_{CC}, and V_{DD} are the variable supply voltages for the D-RAM being tested. V_{DD} is the voltage applied to the field electrodes.

The element being tested is mounted on a test head. The test head is connected to the memory tester by a pair of 16 conductor ribbons. Some shielding was obtained

11. Lockhart, Jim, "Speed Up 4K or 16K RAM Evaluation," Memory Systems Design and Applications, p 225, Dave Bursky (ed) Hayden, Rochelle Park, NY 1980.

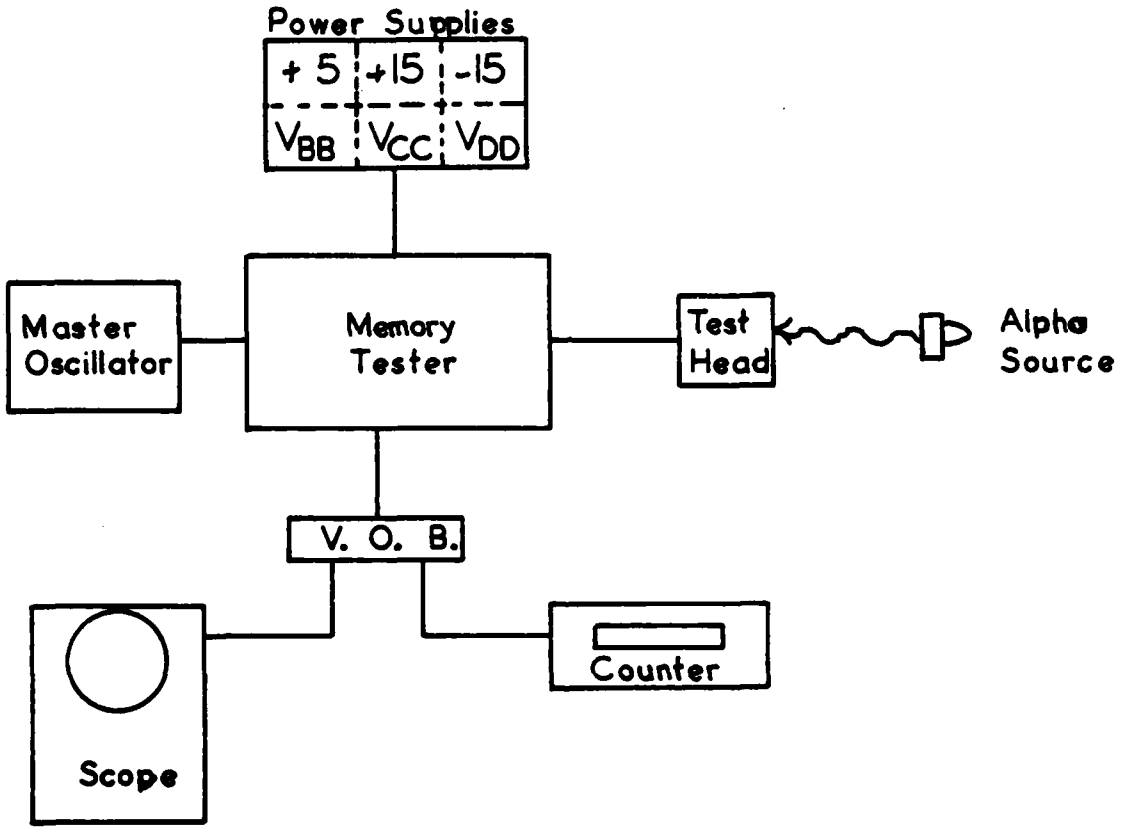


FIGURE 6. 4K-16K EXPERIMENT

by grounding alternate conductors in these ribbons. The only active device on the test head is a 74128 line driver used to transmit the data read out of the memory back to the tester.

The D-RAMs are organized in terms of rows and columns. The 16K element is 128 rows by 128 columns. To reach a cell the binary number of the desired row is latched into the D-RAM then, using the same set of address lines, the binary number of the column is latched in. At this point the individual cell so addressed can be read or written into. The test set-up provides a means to display bits on an oscilloscope as z-axis modulation of a row-column display. The row-column display is generated by a pair of Hybrid Systems, Model 395-12C Digital to analog converters. These are fed with the binary row and column numbers of the cell being addressed. The converters, a delay line and line driver for the z-axis signal are mounted on the video output board (VOB). The digital-to-analog converters feed the x- and y- amplifiers of a Tektronix type 545B oscilloscope. The line driver is connected to either the z- input of the scope or it can be connected to a Monsanto 113A counter-timer when counting errors.

A functional block diagram of the memory tester is shown in Figure 7. The heart of the tester is the 14 bit binary counter which is driven at the clock rate through the timing generator. Omitted for clarity is a pre-multiplexer which changes the system from 16K to 4K by using only the 12 lowest bits in the counter. The output of the counter is the binary address of the particular cell in the memory being addressed. The seven (six for 4K) least significant bits are the row address of the individual memory cell. The seven (six for 4K) most significant are the column address. The address multiplexer (ADD MUX) switches the lines going to the line drivers from the row to the column address lines in response to the AAM signal. Latching a row address into the D-RAM refreshes all the cells with that row address. Thus, since these are the fastest changing address bits, 16K memory will be refreshed in 2^7 times the clock period; e.g., for a 1 MHz clock in 128 microseconds.

The fourteen address bits also feed a set of display latches, an LED display and a data generator. The display latches drive the digital-to-analog converters on the video output board. The data generator comprising a set of logic gates generates data input to the D-RAM. The data pattern appears on the scope as vertical or horizontal bars or as a checkerboard. The bar width can be selected as 1, 2, 4, 8, 16, or 32 bits wide. The horizontal and vertical width of the checkerboard elements can also be selected from the same range. The unit can also load all zeros or all ones. The error detection and display select section compares the data signal from the data generator with that from the memory chip being tested and sets an error latch if they are different. It can be set to send to the display latch input data, all errors detected, only zero to one errors or only one to zero errors. The interrupt latch can be set to run continuously, stop immediately on error showing the address of the error or stop on error after finishing the cycle of addresses.

We show the steps which occur in a single cycle of the tester in Figure 8, which is a plot of the timing signals which are the output of the timing generator. The rising edge of the clock pulse triggers the timing generator. This immediately triggers the AAM, setting the row addresses into the line drivers and hence onto the memory address lines. Next the $\overline{RAS}$ goes low latching this row address into the memory. The AAM then goes low. This shifts the ADDMUX to the column address bits which are then latched into the memory by $\overline{CAS}$ going low. Next the output data from the memory is latched into the data latch. A NOR gate senses the presence of errors

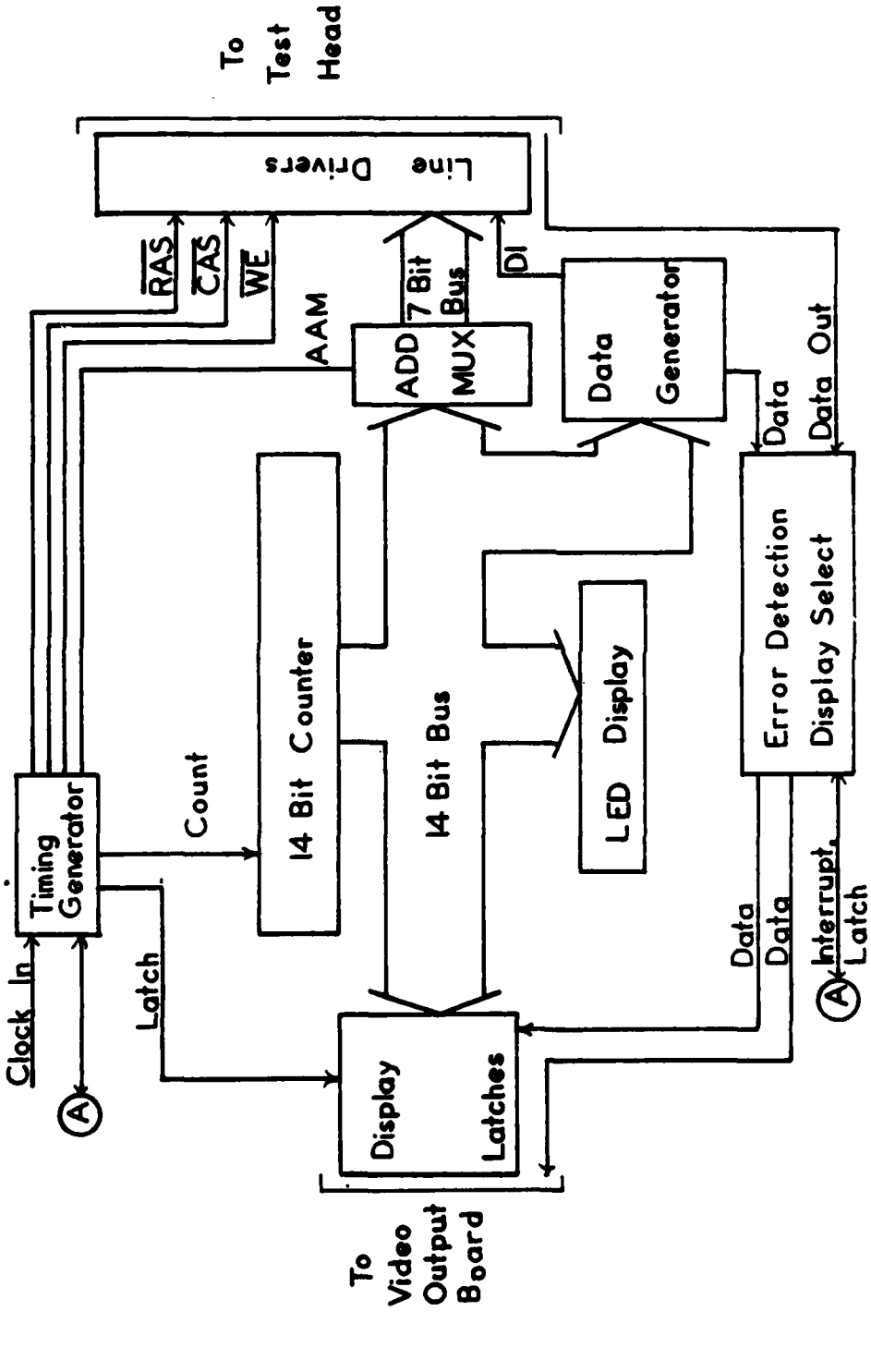


FIGURE 7. MEMORY TESTER BLOCK DIAGRAM

which are then latched into the display (if errors are being displayed). The $\overline{WE}$ goes low which writes into the memory cell the data on the data input line regardless of whether or not an error was detected. Finally the COUNT pulse increments the counter for the next cycle.

There are two outputs, one through the display latches and a second which is a pulse reproducing the Error Latch. The output through the latches is used to drive the z-axis of the scope. The pulse output is used to drive the counter. Note that if one tried to drive the counter off of the display latches two consecutive errors would only be counted as one.

THE 4K-16K EXPERIMENTAL RESULTS

Using the set-up described above we detected alpha particles using a Texas Instruments 4116 D-RAM. We removed the cover with the same technique used on the 64K RAM and mounted the exposed chip in the test head. A very weak Thorium source was placed over the chip and error counts were recorded.

At the designed operating voltage the memory was insensitive to alpha particles. However, as we reduced V_{DD}, which is the field electrode voltage a range was reached in which the alpha source caused errors. These data are shown in Figure 9. Above about eight volts this memory was insensitive to alphas. The rated voltage for this memory is twelve volts. Below about six volts the memory gives a large number of errors, in the absence of the source. We term this the breakdown region and assume that there, V_{DD} is so low that the cells do not hold enough mobile charge to actuate the sense amplifiers and hence will not store data. In between there is about a two volt range in which the memory counts alpha particles. The data points in the figure each represent five minutes counting. A zero run with the source removed from the test head resulted on no counts in half an hour.

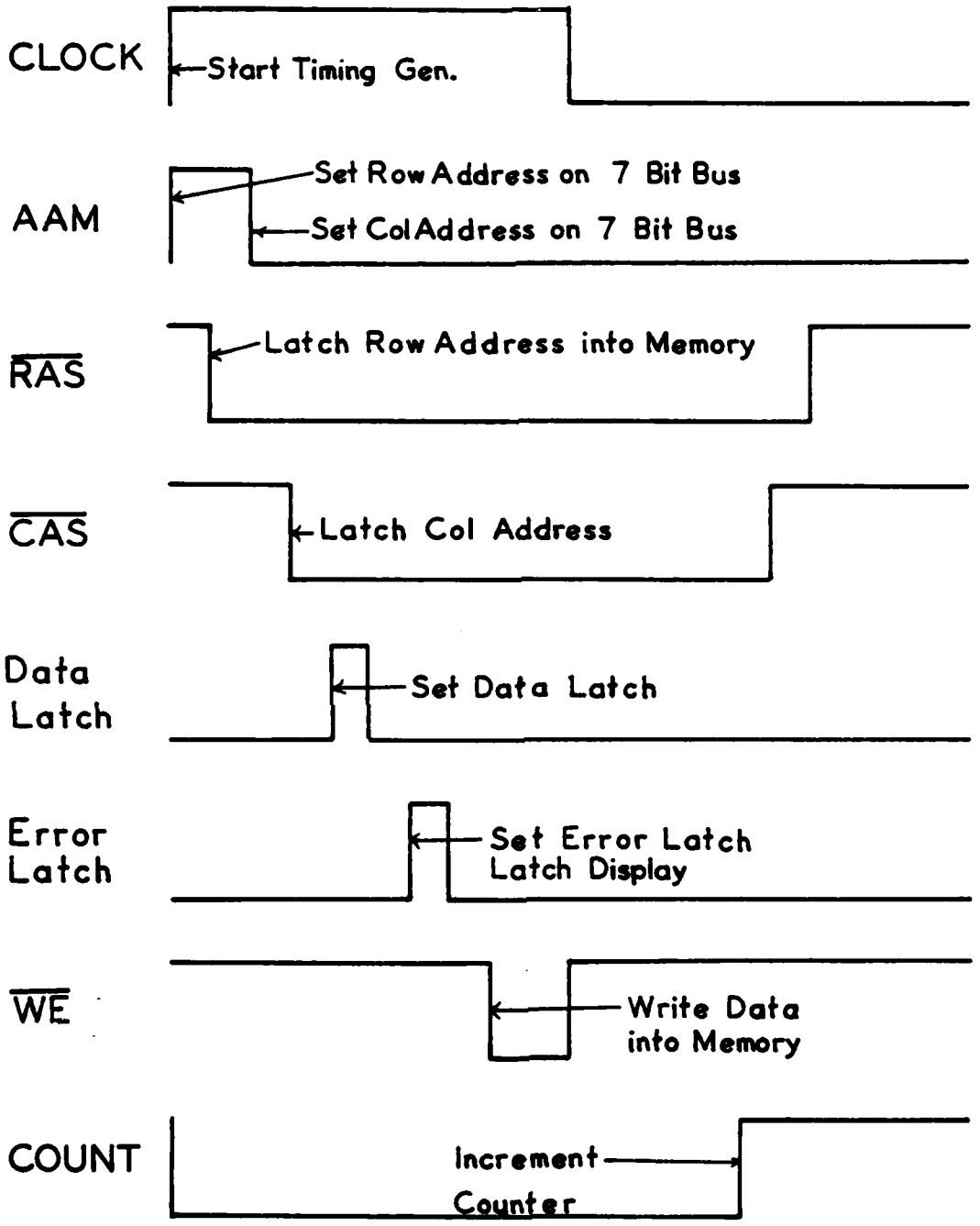


FIGURE 8. MEMORY TESTER TIMING SIGNALS

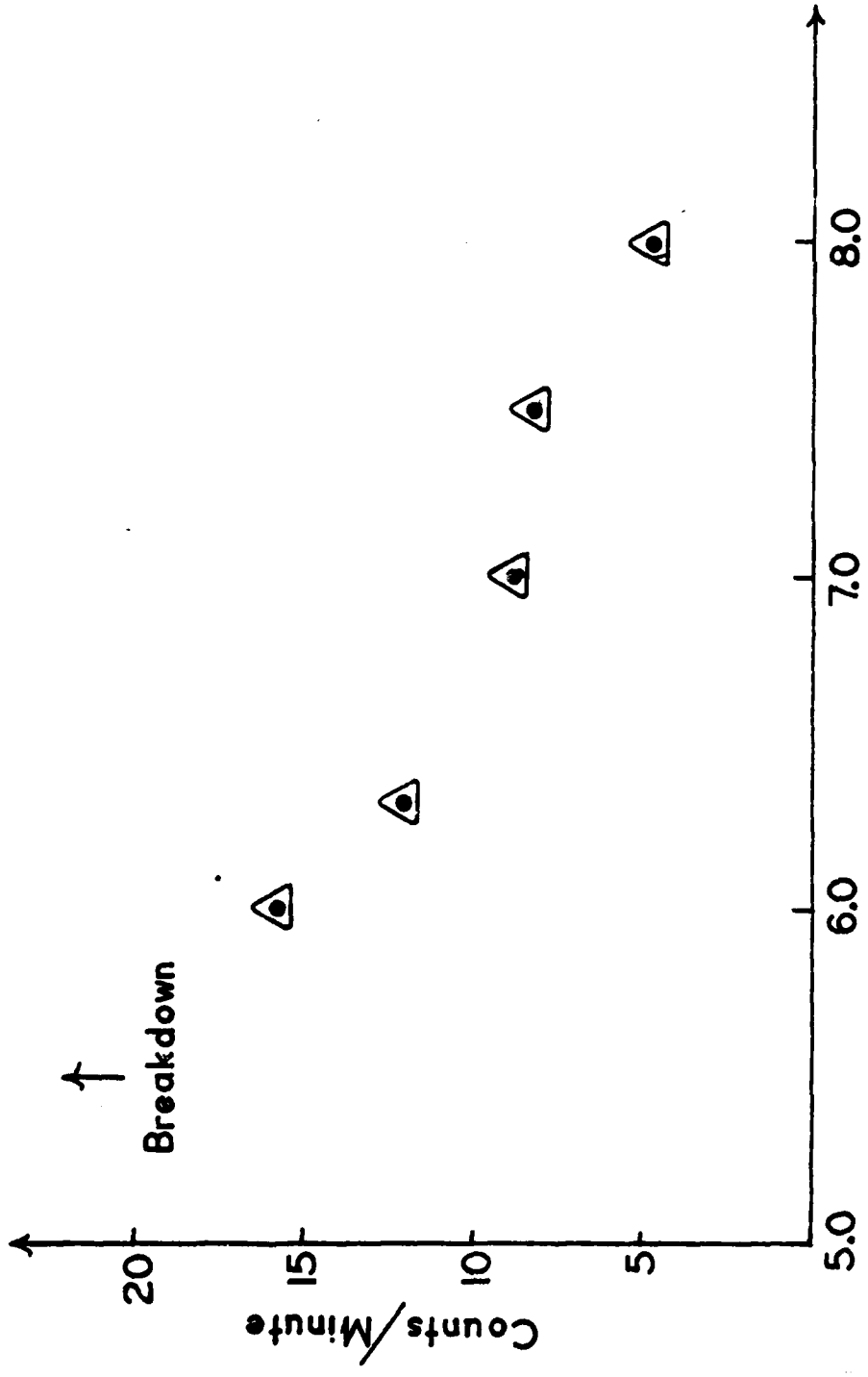


FIGURE 9. COUNTING RATE VS V_{DD} TI 4116 D-RAM

CHAPTER 3

CONCLUSIONS AND RECOMMENDATIONS

The primary conclusion to be drawn from the experiments described in this report is that commercially available D-RAMs can function as counters of alpha particles. Further, they can be incorporated into standard digital circuits which can then be used to accumulate total count and to calculate current dose rate. Thus the basic feasibility of a digital dosimeter has beem demonstrated.

Further research should be directed to the incorporation of the D-RAMs into a practical dosimeter. A primary question is how to make the D-RAM sensitive to fast neutrons. The most likely solution would be to devise a radiator or moderator which would convert the neutron to radiation to which the D-RAMs would respond. Two possibilities are immediately apparent: first, generating high energy protons by elastic collisions in a hydrogen bearing moderator and second, generating alpha particles by thermalizing the neutrons in a hydrogen bearing moderator and then absorbing the neutrons in boron with the subsequent emission of an alpha. These two moderators should be built and the sensitivity of the resulting detector determined quantitatively. In addition enough D-RAMs of both types should be tested to establish the variation in alpha sensitivity for each type. Other devices (such as CCDs) should also be tested as potential detectors. Finally, an optimized design should be developed.

REFERENCES

1. Brackenbush, L. W., and Endres, G. U., "Personnel Neutron Dosimetry at Department of Energy Facilities," Pacific Northwest Laboratory Report PNL-3212, UC-41, August 1980. Available from NTIS, 5285 Port Royal Road, Springfield, VA 22151.

2. May, Timothy C., and Woods, M. H., "A New Physical Mechanism for Soft Errors in Dynamic Memories," Proc. 16th Annual Conference on Reliability Physics, IEEE, New York, 1978 p. 33.

3. Bouldin, D., and Kumar, A., "Materials Analysis Aspects of the Alpha Particle Induced Error Phenomenon," Proc. 29th Electronics Components Conf., IEEE New York, 1979, p. 265.

4. Gibbons, H. P., and Pittman, J. D., "Alpha Particle Emissions of Some Materials in Electronic Packages," Proc. 29th Electronics Components Conf., IEEE, New York, 1979, p. 257.

5. Guenzer, C. S., Wolichi, E. A., and Allas, R. G., "Single Event Upset of Dynamic Rams by Neutrons and Protons," IEEE Trans. on Nuclear Sci., NS-26(6), 5048 (Dec. 1979).

6. Wyatt, R. C., McNulty, P. J., Toumbas, P., Rothwell, P. L., and Fily, R. C., "Soft Errors Induced by Energetic Protons," IEEE Trans. on Nuclear Sci., NS-26(6) 4905(Dec. 1979).

7. Campbell, A. B., and Wolichi, E. A., "Soft Upsets in 16K Dynamic RAMs Induced by Single High Energy Protons," IEEE Trans. Nuclear Sci., NS-27(6), 1509(Dec. 1980).

8. Sivo, L. L., Peden, J. C., Brettschneider, M., Price, W., and Pentecost, P., "Cosmic Ray Induced Soft Errors in Static M.O.S. Memory Cells," IEEE Trans. on Nuclear Sci., NS-26(6), 5042(Dec. 1979).

9. Yaney David S., Nelson, J. T., and Vansskike, Lowell L., "Alpha Particle Tracks in Silicon and Their Effect on Dynamic M.O.S. Reliability," IEEE Trans. on Electron Devices ED-26(1), 10(Jan. 1979).

10. Cerofolini, Gianfranco, and Ferla, Giuseppe, "A Proposal: Dynamic RAMs as Particle Detectors," Nuclear Instruments and Methods, 169, 125(1980).

11. Lockhart, Jim, "Speed Up 4K or 16K RAM Evaluation," Memory Systems Design and Applications, p. 225, Dave Bursky (ed) Hayden, Rochelle Park, NY 1980.

DISTRIBUTION

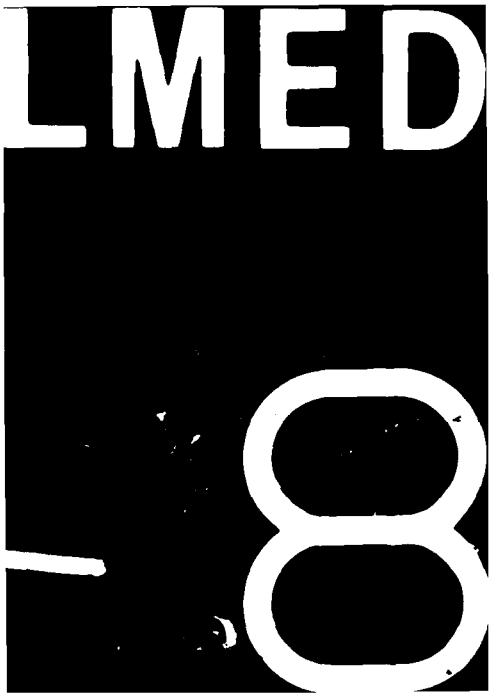
	Copies
Chief of Naval Operations Attn: OP455 (CDR K. H. Thomas) Washington, DC 20350	1
Naval Electronic Systems Command Attn: Code 8153 (LCDR M. Elkins) Washington, DC 29360	1
Naval Sea Systems Command Attn: Code 644 (CDR Ken Groves) Washington, DC 20360	1
Naval Sea Systems Command Attn: Code 06R Washington, DC 20362	1
Headquarters, Department of Army DCS Ops & Plns Attn: DAMO-NC Washington, DC 20310	1
U.S. Department of Energy Assistant Secretary for Environment Washington, DC 20545	1
U. S. Department of Energy Director, Operational & Environmental Safety Division Washington, DC 20545	1
U.S. Department of Energy Director, Office of Environmental Compliance & Overview Washington, DC 20545	1
U.S. Department of Energy INRAD Attn: CDR Frank Glockner Mail Stop A362 Germantown Washington, DC 20545	4
U.S. Department of Energy Deputy Assistant Secretary for Research Washington, DC 20545	1
U.S. Department of Energy Chief, Health Protection Branch Operational & Environmental Safety Division Washington, DC 20545	1
U.S. Department of Energy DOE/OMA DP-20 (GTN) A-362 Attn: John Taylor Washington, DC 20545	1
U.S. Department of Energy Manager, Health Physics Program Operational & Environmental Safety Division Washington, DC 20545	1
U.S. Department of Energy Director, Operational Safety Division Albuquerque Operations Office P.O. Box 5400 Albuquerque, NM 87115	1
U.S. Department of Energy Director, Operational & Environmental Safety Division Chicago Operations Office 9800 South Cass Avenue Argonne, IL 60439	1
U.S. Department of Energy Operations Branch Chief Dayton Area Office P.O. Box 66 Miamisburg, OH 45342	1

	Copies
U.S. Department of Energy Assistant Manager, Environmental Safety & Health Programs Idaho Operations Office 550 Second Street Idaho Falls, Idaho 83401	1
U.S. Department of Energy Chief, Operational Safety Section Kansas City Area Office P.O. Box 202 Kansas City, Missouri 64141	1
U.S. Department of Energy Health & Safety Coordinator Los Alamos Area Office 528 Thirty-Fifth Street Los Alamos, New Mexico 87544	1
U.S. Department of Energy Director, Office of Safety & Health Nevada Operations Office P.O. Box 14100 Las Vegas, Nevada 89114	1
U.S. Department of Energy Director, Safety & Environmental Control Division Oak Ridge Operations Office P.O. Box E Oak Ridge, Tennessee 37830	1
U.S. Department of Energy Chief, Safety & Environment Branch Rocky Flats Area Office P.O. Box 928 Golden, Colorado 80401	1
U.S. Department of Energy Attn: A. R. Sneddon, Jr. Sandia Area Office P.O Box 5400 Albuquerque, New Mexico	1
U.S Department of Energy Director, Environment, Safety & Program Support Division San Francisco Operations Office 1333 Broadway Oakland, California 94612	1
U.S. Department of Energy Director, Safety & Environmental Division Savannah River Operations Office P.O. Box A Aiken, South Carolina 29801	1
U.S. Department of Energy Attn: F. Hajnal Environmental Measurements Lab. 376 Hudson Street New York, NY 10014	1
U.S. Department of Energy Attn: W. Lowder Environmental Measurements Lab 376 Hudson Street New York, NY 10014	1
U.S. Department of Energy Attn: J. E. McLaughlin Environmental Measurements Lab 376 Hudson Street New York, NY 10014	1
U.S. Department of Energy Attn: J. P. Cusimano Health Physics Lab P.O. Box 2108 Idaho Falls, ID 83401	1
U.S. Department of Energy Attn: T. J. Glasson Knolls Atomic Power Lab P.O. Box 1072 Schenectady, NY 12301	1
U.S. Department of Energy Attn: J. F. Koury Pittsburgh Naval Reactors Office P.O. Box 109 W. Mifflin, PA 15122	1
U.S. Department of Energy Attn: D. J. Hamilla Schenectady Naval Reactors Office P.O. Box 1069 Schenectady, NY 12301	1

	Copies
U.S. Department of Energy Attn: D. E. Jones Bldg. CF 690 550 Second Street Idaho Fall, Idaho 83401	1
U.S. Nuclear Regulatory Comm. Chief, Occupational Health Standards Branch Washington, DC 20555	1
U.S. Nuclear Regulatory Comm. Attn: Seymour Block Environmental Evaluation Branch Division of Operating Reactors Washington, DC 20555	1
U.S. Nuclear Regulatory Comm. Attn: J. Foulke 7915 Eastern Avenue, Room 1014 Silver Spring, MD 20555	1
U.S. Nuclear Regulatory Comm. Attn: H. J. Pettengill Rockville, MD 20850	1
Iowa State University Attn: M. D. Voss Ames Laboratory Ames, Iowa 50011	1
Argonne National Laboratory Attn: E. H. Dolacek 9700 South Cass Avenue Argonne, Illinois 60439	1
Argonne National Laboratory Attn: D. P. O'Neil 9700 South Cass Avenue Argonne, Illinois 60439	1
Argonne National Laboratory Attn: C. S. Abrams Idaho Site P.O. Box 2528 Idaho Falls, Idaho 83401	1
Bettis Atomic Power Laboratory Attn: W. R. Harris P.O. Box 79 West Mifflin, PA 15122	1
Bettis Atomic Power Laboratory Attn: R. M. Muzik P.O. Box 79 West Mifflin, PA 15122	1
Brookhaven National Laboratory Attn: V. P. Bond Upton, NY 11973	1
Brookhaven National Laboratory Attn: C. B. Meinhold Safety & Environmental Protection Division Upton, NY 11973	1
E. I. duPont de Nemours & Co. Attn: H. P. Boiter Health Physics Department Savannah River Plant Aiken, SC 29801	1
Fermi National Accelerator Laboratory Attn: L. M. Lederman P.O. Box 500 Batavia, Illinois 60510	1
Fermi National Accelerator Laboratory Attn: A. L. Read P.O. Box 500 Batavia, Illinois 60510	1
Fermi National Accelerator Laboratory Attn: S. Velen P.O. Box 500 Batavia, Illinois 60510	1
General Electric Company Attn: E. P. Forest Neutron Devices Dept. P.O. Box 11508 St. Petersburg, Florida	1
Lawrence Berkeley Laboratory Attn: J. McCaslin Bldg. 75B 1 Cyclotron Road Berkeley, CA 94720	1
Lawrence Livermore Laboratory Attn: R. V. Griffith P.O. Box 808 L-520 Livermore, CA 94550	1

	Copies
Lawrence Livermore Laboratory Attn: D. E. Hankins P.O. Box 808 L-520 Livermore, California 94550	1
Los Alamos Scientific Laboratory Attn: J. E. Dummer Health Physics Group Los Alamos, New Mexico 87545	1
Los Alamos Scientific Laboratory Attn: J. N. P. Lawrence MS-401 Los Alamos, New Mexico 87545	1
Los Alamos Scientific Laboratory Attn: G. L. Voelz P.O. Box 1663 Los Alamos, New Mexico 87545	1
Lovelace ITRI Attn: R. Taylor P.O. Box 5890 Albuquerque, New Mexico 87115	1
Monsanto Research Corporation Attn: P. C. Adams P.O. Box 32 Miamisburg, Ohio 45342	1
Oak Ridge Gaseous Diffusion Plant Attn: J. C. Bailey P.O. Box P Oak Ridge, Tennessee 37830	1
Oak Ridge National Laboratory Attn: J. A. Auxier P.O. Box X Oak Ridge, Tennessee 37830	1
Rockwell International Attn: E. Putzier Rocky Flats Plant P.O. Box 464 Golden, Colorado 80401	1
Sandia Laboratories Attn: W. D. Burnett P.O. Box 5800 Albuquerque, New Mexico 87115	1
Stanford Linear Accelerator Attn: D. D. Busick P.O. Box 4349 Stanford, California 94305	1
Union Carbide Corporation Attn: J. D. McLendon P.O. Box Y Oak Ridge, Tennessee 37830	1
Pacific Northwest Laboratory Attn: William Bair L. W. Brackenbush William Glass P.O. Box 999 Richland, Washington 99352	1 1 1
National Bureau of Standards Attn: Randy Coswell Building 245 - Rm. B102 Washington, DC 20234	1
Sandia Laboratories Livermore Attn: Perry Lovell Div. 8275 P.O. Box 969 Livermore, California 94550	1
DELET-ER Electronic Technology and Development Laboratory Attn: Stanley Kronenberg Fort Mammoth, New Jersey 07703	1
EG&G-Santa Barbara Attn: William Quam P.O. Box 98 Goleta, California 93017	1
University of California, L.A. Attn: Jim Smathers Department of Radiation Oncology Center for the Health Sciences Los Angeles, California 90024	1
University of Wisconsin Attn: Paul DeLuca 3321 Sterling Hall Madison, Wisconsin 53706	1

	Copies
Yale University Attn: Robert Apfel P.O. Box 2159 New Haven, Connecticut 06520	1
University of Lowell Attn: Dr. George C. Chobat One University Avenue Lowell, Massachusetts 01854	1
Defense Technical Information Center Cameron Station Alexandria, VA 22314	2


LMED
8